Low Cost Flip Chip (LCFC): An Innovative Approach for Breakthrough Reduction in Flip Chip Package Cost

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Abstract

A new low cost flip chip (LCFC) packaging solution is developed that dramatically reduces flip chip package cost. The solution entails innovations and improvements in the bump, interconnect structure, substrate design and underfilling process. Cu column bumps with solder caps are used to form a "Bump on Lead (BOL)" interconnection with narrow substrate pads with no solder mask confinement ("open solder mask", or "open SR") and no solder-on-pad finish ("no SOP"). This results in a substrate design with relaxed design rules despite high I/O escape densities, enabling a majority of IC designs in the sub-1000 pin range to fit in 2-lyr laminate substrates. The novel BOL/open SR/no-SOP interconnect structure is combined with a mold underfilling (MUF) process using high density 1-up matrix substrates to achieve high substrate utilization and low process cost. Furthermore, it is shown through empirical data and FEA modeling that the unique mechanical structure of the BOL interconnection remarkably reduces the stress on Si sub-surface layers resulting in elimination of the low K damage phenomenon commonly observed in sub-45 nm Si nodes. The LCFC technology is Pb-free, scalable to very fine pitch in the sub-100 um range and highly electromigration-resistant, providing a natural migration path to 3D/TSV micro bump / micro bond and green solutions for the future. In the present paper, we present in detail, the structure, assembly process and reliability of this packaging solution. We also present data on the application of the solution to advanced sub-45 nm Si nodes with ELK (Extra Low K) dielectrics.

1. Introduction

The convergence of traditional computing systems (such as PC's, Notebook computers and Game consoles) and mobile hand held products (such as cellular phones) is an inevitable trend in the Electronics industry. This trend will drive the need for what may be called the "holy trinity" of performance, form factor and low cost. The development of low cost flip chip packaging solutions is a step in this direction.

While it is well understood that flip chip packaging will provide the optimum solution in the "convergence space" described above, the significant gap in cost compared with the incumbent wire bond solution has been a barrier to proliferation (and subsequent cost erosion through economies of scale). Hence, we believe it is important to target cost parity with wire bond packaging as an essential factor to enable adoption. Along these lines, we have performed a detailed analysis and comparison of package cost between wire bond and flip chip packaging. The result is summarized in fig 1.1, which is based on an average case of fcFBGA and fcBGA packages in the 150 – 1000 pin count range. It is evident that for a wire bond package, the substrate and the wire bonding each comprise approximately 40 % of total cost (for a total of 80%) with other elements only adding up to ~ 20%; when this is compared with a traditional flip chip package for the same application, the total cost is increased by ~ 35%, most of which comes from the premium required for the Build-up substrate which is inevitably necessary to achieve the escape routing in case of a flip chip area array interconnection. Hence, our approach has been to develop fundamental improvements that strike at the substrate cost element with concomitant improvements in other areas. As is clear from the third bar in fig. 1.1, the proposed LCFC solution does just that: it enables the use of low cost substrates which takes away the substrate premium as a major impact factor for cost and applies other accompanying improvements like MUF for further reductions. In this way, we have demonstrated a flip chip solution that, for any given application, provides a cost point well below that for the corresponding wire bond solution for the same application. We anticipate that this innovation will enable widespread adoption of flip chip packaging in the "convergence" space alluded to above also resulting in subsequent further cost erosion through economies of scale.

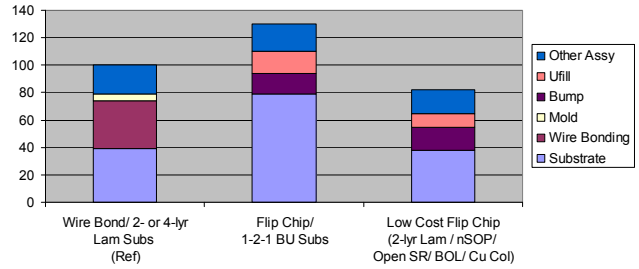


Fig. 1.1 Cost structure of wire bond and flip chip packaging

2. Key Elements of Low Cost Flip Chip (LCFC)

Our approach for reduction of flip chip package cost is depicted in Fig. 2.1. In line with the cost analysis framework shown in section 1, our strategy was to focus on the substrate, underfill and other process costs in that order of emphasis.

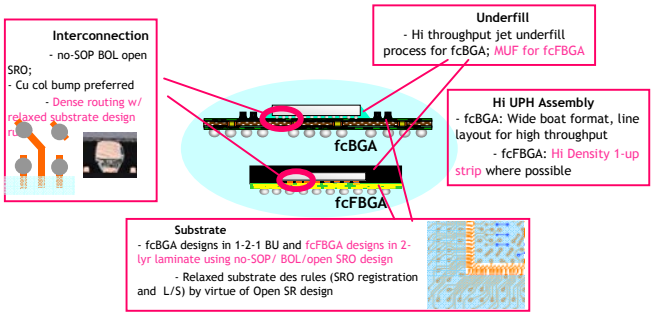
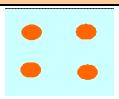


Fig. 2.1: Approach for flip chip package cost reduction

The biggest impact comes from an innovative interconnect structure termed "no-SOP/BOL/Open SRO" which enables dramatic improvement in escape routing density with relatively coarse substrate design rules. The interconnect structure and associated improvement in routing density are schematically illustrated in Table 2.1. We have shown typical substrate design rules and escape densities achieved using conventional Build-up substrates with SMD –SOP (Solder Mask Defined - Solder on Pad) pad configuration vs. 2-lyr laminate substrates with no-SOP and open SR pad configuration. The escape routing density is expressed in terms of effective escape pitch and # of routable I/O for a presumed case of an 8 x 8 mm die (selected for the purpose of illustration). It is evident that for a typical case as illustrated, the new interconnect structure achieves higher routing densities with far more relaxed substrate design rules compared to a conventional 1-2-1 BU substrate. Our analysis of I/O densities of actual devices shows that > 60% of IC designs spanning the gamut from GPU/CPU, Chipset, FPGA, ASIC and RF/Analog can be routed in 2-lyr laminate substrates from a point-to-point routing perspective based on the design rues illustrated in Table 2.1. It should be clear that the new structure can be used either for achieving higher routing densities for a given set of design rules or conversely for relaxing the design rules for a given density. The attainment of this higher routing density / design rule simplification with the new interconnect structure is attributable to two key features: (i) the BOL feature [(1)] which allows narrowing of the substrate pad thereby opening up space for routing of adjacent traces (ii) the "Open SR" feature which essentially obviates the use of solder mask for confining solder flow thereby eliminating the routing space otherwise used up to account for tolerances in solder mask opening size and its registration to the metal pattern. The first feature results in a highly asymmetric interconnect geometry (with the bump UBM size significantly greater than the BOL pad width); as is shown later, not only is this structure highly reliable but it helps reduce the mechanical stress propagated into the Si inner layers and is shown to dramatically eliminate damage to low K and ELK layers in new Si nodes. The second feature is made possible by the unique phenomenon of "self confinement" (fig. 2.2) i.e. the design of the bump diameter and size of solder cap in the Cu column bump in conjunction with the geometric dimensions of the substrate pad promotes a condition wherein the molten solder is retained or confined within the space between the non-fusible portion of the bump and the substrate pad by virtue of surface tension forces. As such, the solder "self-fillets" to form a natural solder joint without the need of solder mask to confine its flow. In addition to the routing density benefit, there is additional substrate cost reduction achieved through the elimination of SOP finish on the substrate – this is a significant factor especially at interconnection pitch below 150 um wherein special processing is required to achieve reasonable yields for SOP fabrication.

		1-2-1 BU SMD-SOP	2-lyr Laminate nSOP BOL/Open SR, Cu Col*
		 20/20 um L/S +/- 25 um SR registrn 80 um SRO 120 um via cap pad	 35/40 um L/S open SR 350 um via cap pad
Bump Pitch (um)		190 um	150 um
I/O Density	Effective pitch	95 um	75 um
	# Routable I/O*	481	560
% of real IC designs that "fit" in stated des rules		40%	> 65%
Cost Impact	Substrate	1.0 X	0.48 X
	Package	1.0 X	0.72 X

* assumes 8 x 8 mm die and fcFBGA package with 0.5 mm terminal pitch

Table 2.1: Design rule and I/O density comparison

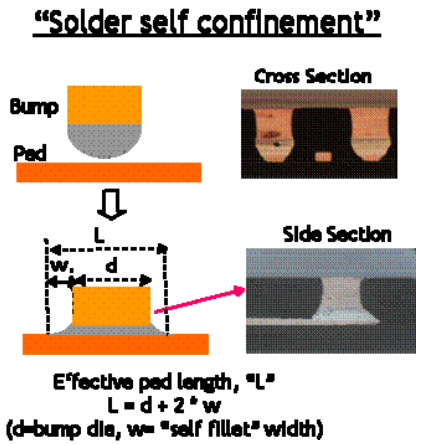


Fig. 2.2: Illustration of solder self confinement

The second key aspect of LCFC is the replacement of conventional capillary underfilling with mold underfilling (MUF) which results in additional cost reductions in the assembly process. MUF was proven out in conjunction with the innovative interconnect structure described above (see section 4).

Last but not the least, we developed optimized matrix strip formats for processing the flip chip devices which provide higher utilization (greater # of units per strip and a net higher # of units per substrate panel) such as wide strip formats and 1-up molding i.e. no segments in the molded regions of a strip. This approach has resulted in reduction of per unit substrate and processing costs due to a larger # of units being processed at the same time.

3. Test Vehicle Description

Two packages were used for assembly process characterization and reliability testing. They are referred to as "LCFC TV2" and "CP TV", the former being a passive daisy chain (DC) device and the latter a live 65 nm low K product. The design features of die and package are summarized in Table 3.1. Images of bump pattern and substrate top bump pad layer of TV2 are shown in Fig 3.1 and a schematic of the Cu column bump structure used is shown in Fig. 3.2. The TV2 is a 1-metal daisy chain die, while the CP TV is a functional Si device typical of a 65 nm low K Si fab process.

Package Design Features	LCFC TV2	CP TV
Si Node	1L DC die	65nm
Die Size (mmxmm)	8x8	5.3x5.4
Package Size (mm)	12x12	10x10
Bump Alloy	Sn2.5Ag	Sn2.5Ag
# of Bump / Balls	689 / 560	515 / 384
Bump Pitch at Outer Bump	150 um	150um
# of Substrate Layers	2L	4L
Substrate Core Thickness (um)	150	60
Min External Trace Width / Gap	35/40um	20/20um
BGA Ball Pitch (um)	400	400

Table 3.1 Summary of design features of the Test Vehicles

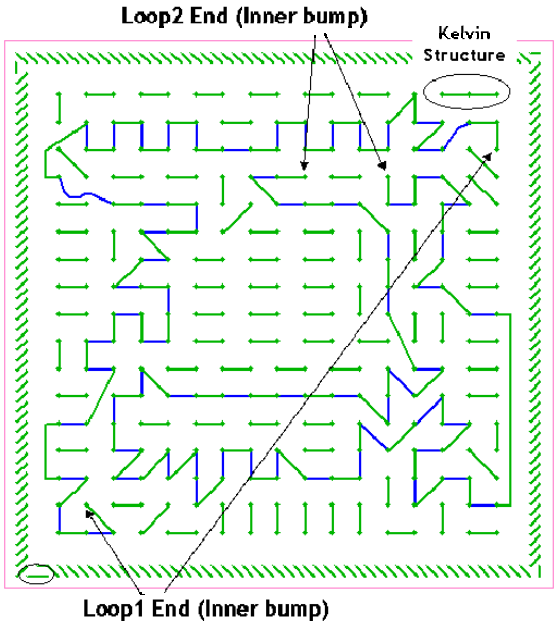


Fig. 3.1 (a)

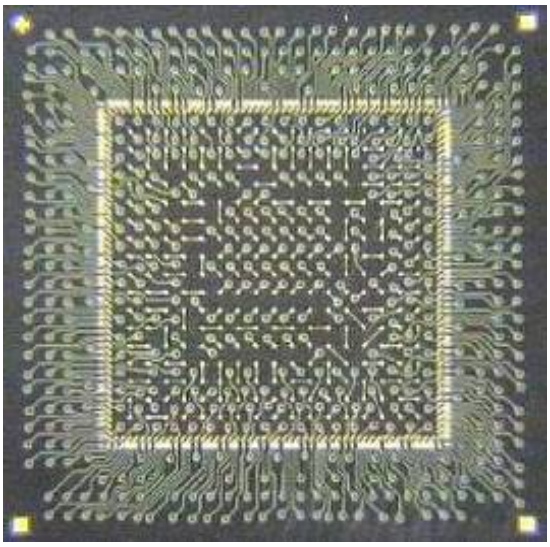


Fig. 3.1 (b)

Fig. 3.1 (a) Schematic of daisy chain (DC) stitch pattern where green and blue lines show DC's on die and substrate respectively; (b) optical image of top layer of TV2 substrate

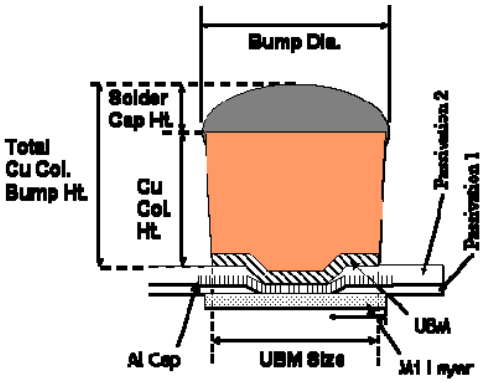


Fig. 3.2 Cross-sectional schematic of Cu column bump

TV2 die was designed to include various features. They include 1) daisy chain connections of outer pads (simulated for I/O pads) and inner pads (simulated for ground and power pads) to detect electrical continuity, 2) various bump pad widths and spaces to adjacent traces to investigate minimum bump pad width and space to adjacent race capability on 1st level interconnection with Cu column bump and BOL bump pad on a substrate, 3) Kelvin structure to measure bump resistance and electromigration.

Fig 3.3 shows schematic of substrate bump pad design. Various bump pad design options (two bump pad widths, five spaces) were investigated to understand their effects on assembly process. Outer row DC chains were designed to measure electrical open and short; while inner DC chains comprised multiple individual daisy chains and two long DC chains. The long DC chains were introduced due to limited space available for all bumps electrically connected to BGA balls on a substrate bottom layer.

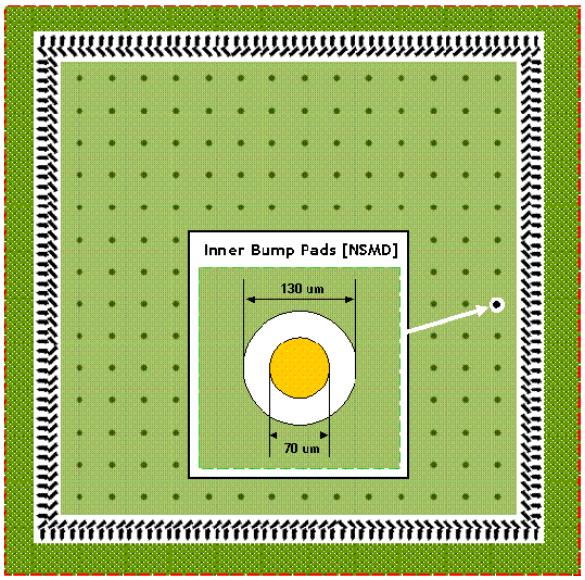


Fig. 3.3

Fig. 3.3 Schematic of substrate bump pad design

4. Assembly Process

Packages were assembled using the same equipment as is typically used in the production of standard fcFBGA

packages with solder bumps and mold underfill (MUF) process.

The schematic of flip chip process flow that was used in this work is shown in Fig. 4.1

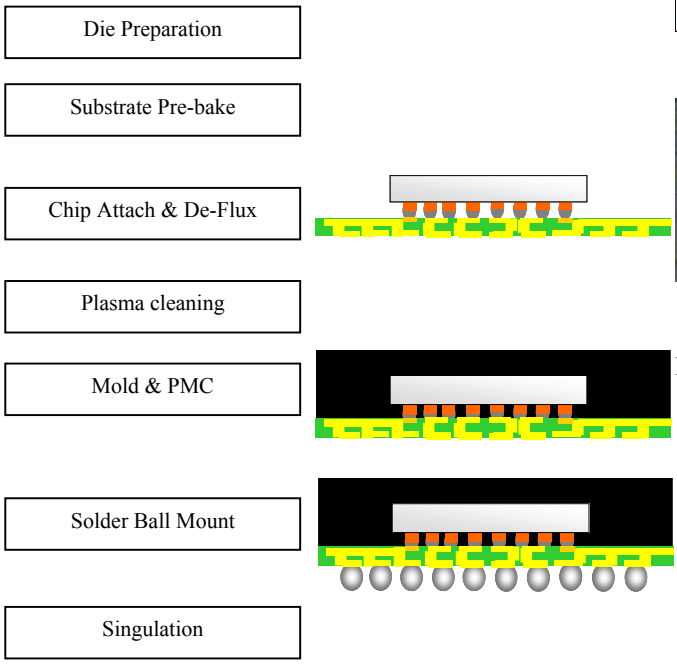


Fig 4.1 Flip chip process flow that was used in this work

Bumped wafers were thinned down to 100um for the 65nm CP TV vehicle and to 200um for the TV2 vehicle. Both vehicles used Cu column bump with solder cap and either 2- or 4-lyr laminate substrates based on BT (bismaleimide triazine) core. After that, chip attach process was performed with attention to several key areas i.e.

- Alignment of Cu column bump and substrate pad
- Bump to adjacent trace shorting
- Solder run out on pad surface

Firstly, to check fine alignment capability, we used the region where the minimum gap between a bump and adjacent substrate trace was 30um. The method consisted of measuring the positional shift after flux dipping and die placement by removal of the die and inspection of the flux footprint and also after chip attach reflow by means of cross sectioning. The different values of intentional positional shift used in the study are shown in Fig 4.2 schematically as well as on the actual substrate pads (the marked area on bump pad represents the shift from nominal position).

In spite of fine space (30um) between bump pad and adjacent trace, shorting to adjacent trace did not occur (Fig. 4.3) even at 20 um shift due to self alignment, although we did detect some offset in the final bonded position for the 20 um shift case. Based on this result, misalignment up to 10 um during chip placement is considered to be comfortably accommodated by means of self alignment.

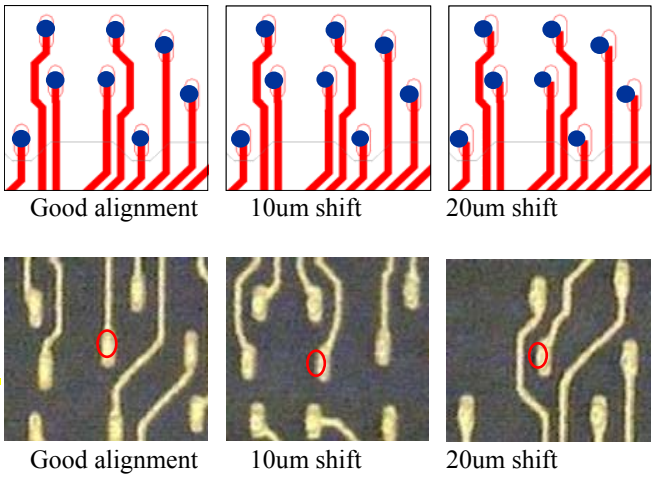


Fig 4.2 Illustration of chip attach positional shift evaluation

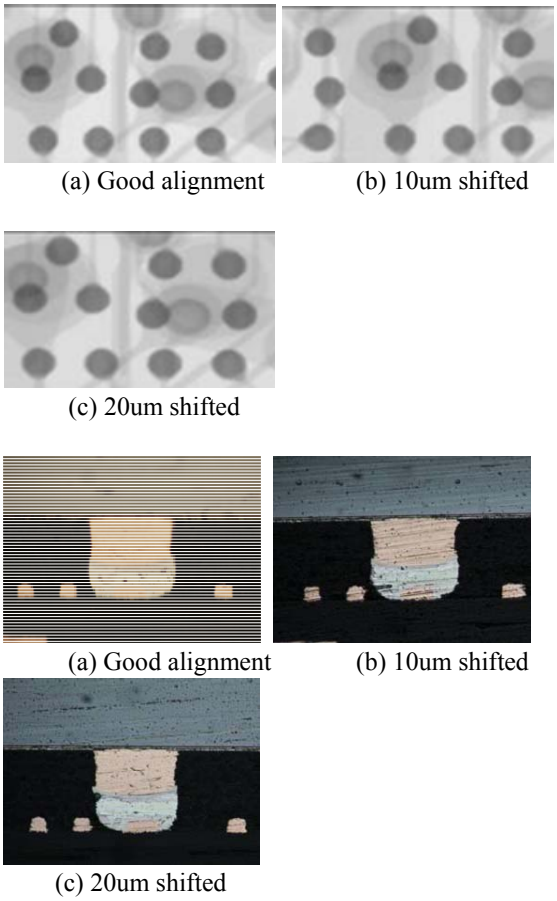
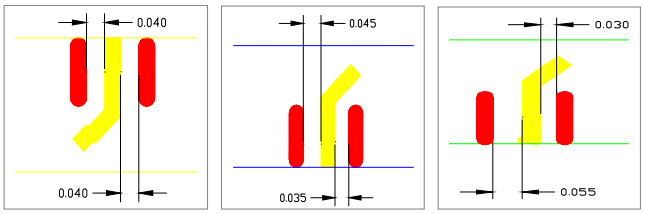


Fig 4.3 X-Ray and X-section images of alignment for various cases of intentional positional shift.

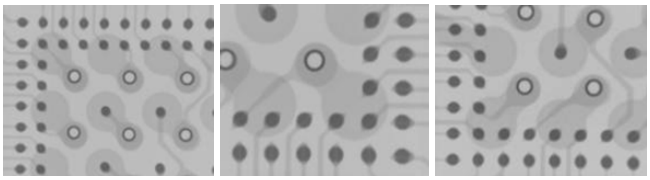
Secondly, we assessed the susceptibility to bump-to-trace shorting more closely using the feature in the TV2 design comprising substrate pads as previously described and depicted in Fig. 4.4.



40um space 35um space 30um space

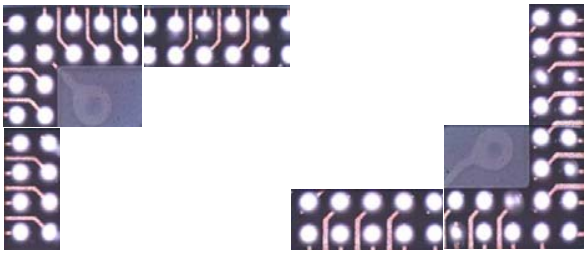
Fig 4.4: Substrate design feature with 40, 35 & 30um space

After the chip attach process, we checked for shorting through X-ray inspection, substrate inspection after die removal and X-section analysis (Fig. 4.5)

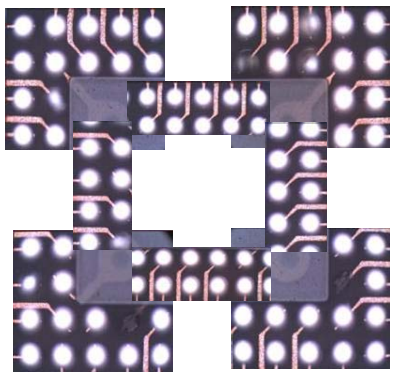


(a) 40um space (b) 35um space (c) 30um space

X-ray inspection images after chip attach



(a) 40um space (b) 35um space



(c) 30um space

Substrate view after chip attach and die removal

(a) 40um space (b) 35um space (c) 30um space

Cross-section view after chip attach

Fig. 4.5 Bump to adjacent trace clearance for various spacings

It was confirmed that no bump to trace bridging occurs up to 30um space while continuing to have no other problems like bump void, non-wet or misalignment.

Finally, both OSP (organic solderability preservation) and ENEPIG (Electroless Nickel, Electroless Palladium & Immersion Gold) finish were evaluated for investigating the effects of solder run out. The chip attach conditions were kept the same as earlier. Fig. 4.6 (a) and (b) show the solder run out for the two surface finishes, (a) for OSP and (b) for ENEPIG.

Fig. 4.6 (a) OSP surface finish

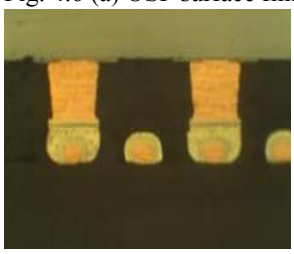
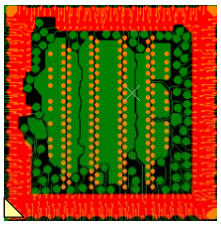


Fig. 4.6 (b) ENEPIG surface finish

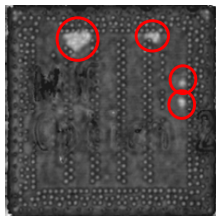
Fig 4.6 Evaluation of solder run-out for OSP & ENEPIG

As is evident from Fig. 4.6, OSP surface finish showed good wet-ability and "self confinement" (no run out) where as the ENEPIG finish shows a limited degree of run out. However, both cases show good wettability with no evidence of marginal solder joint formation. Further optimization of pad geometry / design is needed with ENEPIG finish to achieve a more "self-confined" structure comparable to the OSP case.

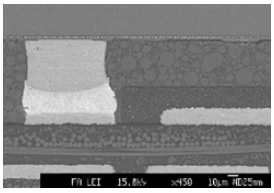
After the chip attach process and flux cleaning steps, the die were underfilled using MUF (molded underfill) technology using a vacuum molding system and 0.45mm mold cap. MUF material and process enable underfill and overmold to be accomplished in one step reducing the assembly process cost significantly. The primary challenges for MUF are consistent filling with no delamination or voiding. To prevent these problems, it is essential to maintain a vacuum profile across the cavity and substrate strip through close control of air vent parameters and flow distribution over the strip area. It is also imperative to select the optimum mold compound that matches the properties of the bump and substrate materials.

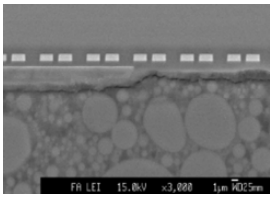


(a) Substrate design



(b) Abnormalities in C-SAM image





(c) Cross-section view of regions shown in (b) above

(d) C-SAM image after optimization of MUF material

Fig. 4.7: Illustration of cracking induced by MUF process

Improper process parameters or poorly optimized mold compound choice can result in MUF-induced voiding, delamination and/or cracking usually detectable through SAT inspection and confirmed through cross sectioning (e.g. Fig. 4.7 b,c). We believe the use of Cu column bumps introduces an additional measure of difficulty by virtue of it's high elastic modulus and somewhat different properties compared with the standard solder bump. So, we developed an MUF material with lower modulus & higher adhesion strength tailored for the Cu column bump to overcome the cracking propensity. In addition to SAT inspection, we also checked for MUF voiding through parallel lapping (P-lapping) technique. Fig. 4.8 is an example of a p-lap image confirming that there is no MUF voiding. Additional work on MUF technology is covered in a separate paper in this conference [2]

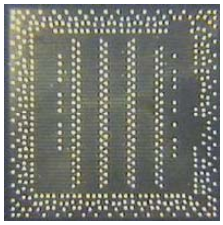


Fig. 4.8: P-lapping image confirming no MUF voiding

The assembly process was completed by performing ball attachment using Pb-free SAC (Sn-Ag-Cu) solder balls of 0.25 mm ball diameter on 0.4 mm pitch on Cu OSP pads.

After the assembly process, construction analysis of the finished pacakge was done by cross section (Fig. 4.9).

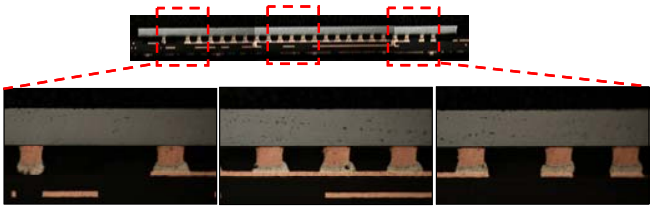


Fig. 4.9: Construction analysis of finished package

For further reduction of substrate and assembly process costs we also developed a process for handling large "High Denisty" (HD) matrix strips with "1-up" molding. The improvement in substrate utilization for an "HD" strip is illustrated in Table 4.2 ("LD" refers to a std. strip and HD to a high density strip).

Table 4.2 Substrate utilization improvement with HD 1-Up

Pkg size	Panel utilization improvemnet
10x10	37.50%
11x11	30.20%
12x12	17.20%
15x15	38.90%

The process was subsequently verified on actual devices and absence of bridging or non-wets, delamiantion, voiding or other defects was confirmed with XRay and SAT inspection (Figs. 4.10, 4.11 and 4.12) . While the initial data is based on a combination capillary underfill + mold process, a simialr verification for a direct mold underfill (MUF) process is currently under way.

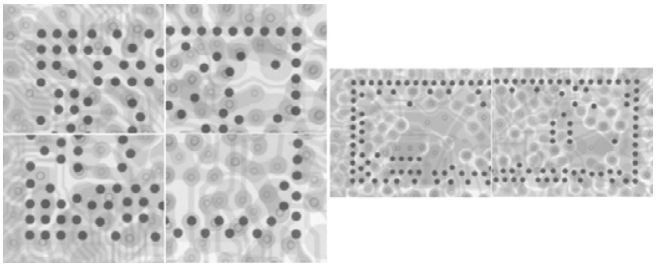


Fig. 4.10: X-Ray image after chip attach reflow

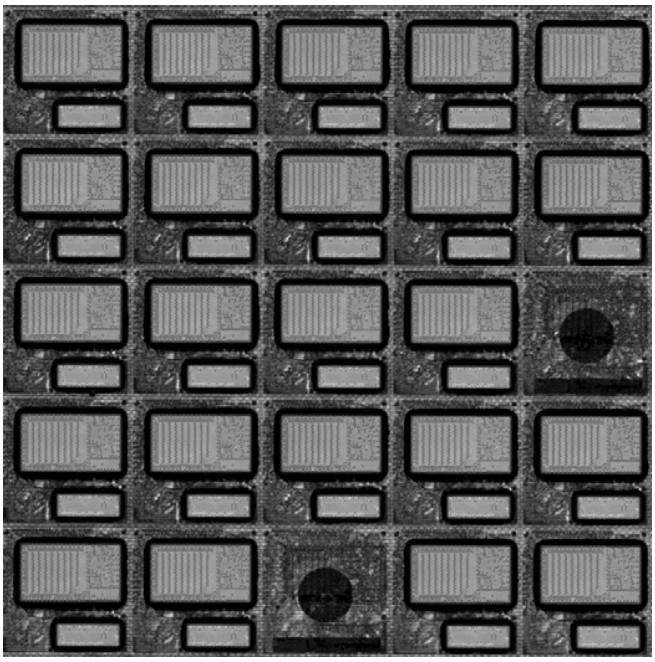


Fig.4.11 : C-SAM void inspection after underfill cure

Fig. 4.12 : Typcial C-SAM image after post mold cure

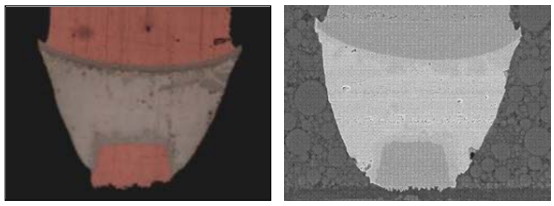
5. Reliability Testing

Table 5.1 gives an overview of the stress conditions used to test the package reliability. The tests are based on JEDEC JESD22- A104-B. Electrical continuity testing was performed to check for Open/Shorts with pass/fail criteria designed to detect leakage or large chagnes in daisy chain resistance. The electical mesurements were made at interim and final readpoints as inidacted in Table 5.1.

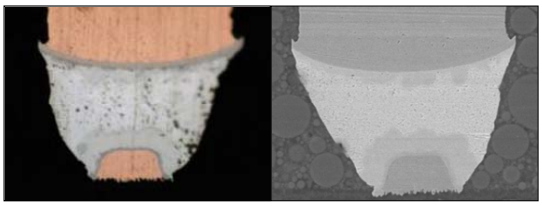
Table 5.1: Stress conditions used for reliability testing

Reliability Test Condition		Min. requirement
Moisture Sensitivity Level	JEDEC Level 1 /2 / 2a / 3 / 4	MSL L3 / 260 ‘C
T/C ‘B’ with Precon	125 ‘C - 55 ‘C / 15 min	500, 1000 cycles
uHAST with Precon	85%RH / 130 ‘C	168hrs
HTST	150 ‘C	500, 1000 hrs

The TV2 as well as the CP TV vehicles passed all relaibilty tests with sufficient margins (tests were typcially extended to 1.5 X of the nominal stress duration to check for margin). In addition to electrical readouts after stressing, post-stress construction analysis was performed to check for wear out modes. There was no evidence of inception of damage in the form of mircocracks or other modes; however, we observed intermetallic gorwth at the Cu – solder interfaces within the interconnection presumably induced by the extended temperature exposure upon extension of the Temp Cycling and High Temp Storage tests. This is illustrated in Fig. 5.1. The intermetallic thickness has increased to ~ 2.5 X it’s original value at the end of assembly. We believe the intermetallic growth is expected and does not pose reliability risk unless the individual intermetallic zones at the two Cu interfaces were to “encroach” potenitally causing brittlenes in the interconnect sturcture. Based on data on hand, we don not anticipate such a phenomenon can occur within the operating life of a real product.



(a) Cross-section imageafter HTST 1500hrs



(b) Cross-section image after TC 1500 cycles

Fig. 5.1: Growth of Cu-Sn intermetallic observed at the Cu-Solder interfaces after extended HTST and Temp Cyl tests

6. Study of LCFC w/ Low K / ELK Si nodes

As has been mentioned previously, the Bond on Lead (BOL) feature of LCFC offers a unique advantage over the more conventional Bond on Capture Pad (BOC) structure due to the more compliant geometry of the resulting solder joint. BOL significantly helps to relieve the stress at the bump-Si interface and hence on the features within the Si thus offering a benefit to flip chip packages with Low K and ELK Si nodes.

The first set of data for the LCFC package with low K Si was obtained using the test vehicle “CP TV” which uses 65 nm low K Si with 150 um bump pitch (Fig. 6.1).

Fig. 6.1: Schematic of 65N-Low K Test Vehicle

In the substrate design, solder resist was removed from the peripheral region (Open SR) to allow fine spaced routing of exposed BOL traces. Solder mask still covered the rest of the die area in the central region. 40u BOL traces were used in Open SR area while 110u pad with 100u SRO in the center

region. Schematic of LCFC substrate top view with BOL in Open SR area is shown in Fig. 6.2.

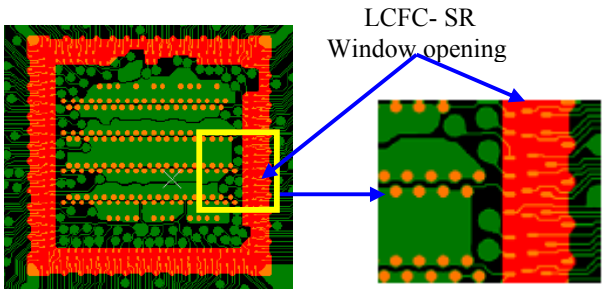


Fig. 6.2: Schematic of LCFC Substrate w/ Open SR and BOL used for 65N Low K test vehicle CP TV

Full qualification of the CP TV test vehicle was completed using 3 lots with 135 units/lot followed by Open/Short and functional testing. Reliability test conditions were similar to those described earlier for test vehicle TV2 (section 5). Qualification results are summarized in Table 6.1.-

Device	LCFC - Package Features	S/S	MSL-L3	uHAST 264hrs	TCB 1000x	HTS 1000hrs
65N-Low K, fcVFBGA	Cu-Column Bump w/ Open SR/BOL Substrate	135 x 3lots	135 x 3lots	45 x 3lots	45 x 3lots	45 x 3lots
Results	Passed					

Table 6.1: LCFC Qualification with 65N-Low K TV.

A separate study was conducted using a 45N-ELK device in a fcVFBGA 13.4 x 13.4 mm package test vehicle with 9.5 x 6.4 mm die and 150u bump pitch. Similar LCFC design with Open SR/ BOL/no-SOP substrate was used to assess impact of LCFC structure on the more fragile ELK dielectric material.

A schematic of the cross sectional view of the test vehicle and top view of LCFC substrate with BOL design are shown in Figure 6.3 and Figure 6.4 respectively.

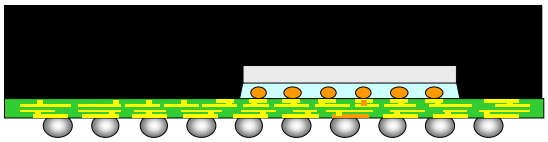


Fig. 6.3: Schematic of 45N-ELK LCFC test vehicle

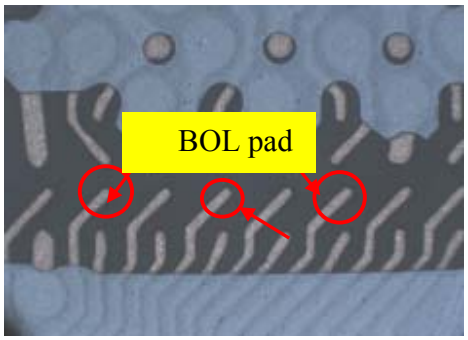


Fig. 6.4: Top view of the substrate showing the Open SR/BOL /no SOP pad design used for 45nm ELK test vehicle.

A systematic study was performed with two different Cu-column designs and BOL substrate pad design using standard SMD-SOP structure as a control leg. C-SAM analysis was used to check for ELK delamination after underfill which is typically revealed by the "white bump" (WB) signature in the C-SAM image. X-ray analysis was also done to check for any non-wetting and solder shorting. The results of the study are summarized in Table 6.2 below. LCFC with BOL design showed promising results with no ELK delamination during the assembly process. By contrast, the control leg using SMD

Table 6.2 45N-ELK LCFC TV Study Results

Leg#	Cu-Column/ LF Solder Cap height	S/S	C-SAM result After WB Reject	Non-wet Inspection	C-SAM result at WB Reject	O/S Reject Result	Remark
1	65%/35%	25	0% (0/25)	20% (1/5)	0% (0/25)	80% (20/25)	LCFC-Open SR with BOL
2	50%/50%	25	0% (0/25)	0% (0/5)	0% (0/25)	0/25	
3		25	0% (0/25)	0% (0/5)	0% (0/25)	0/25	
4		25	0% (0/25)	0% (0/5)	0% (0/25)	0/25	
5	50%/50%	25	28% (7/25)	0% (0/5)	36% (9/25)	0/25	Control-SMD-SOP

SOP substrate pad structure showed a heavy fall-out due to ELK delamination as indicated by White Bump (WB) inspection conducted using C-SAM analysis. It was also found that 45 um Cu column with 35 um solder cap design caused some non-wets. On the contrary, 40u-Cu-column with 40u Solder cap structure proved to be robust. However both structures showed no WB's when used in conjunction with BOL pads. Figure 6.5 shows side-by-side comparison of C-SAM images of BOL legs (Leg#1-4) and BOC leg (#5) showing WB signature only with leg#5.

Fig. 6.5: C-SAM after Chip Attach + UF process of BOL legs and SOP leg showing white Bumps only with SOP leg.

ELK delamination was later confirmed using X-Section analysis of the failed units from Leg#5. The good units from LCFC legs (#1-4) were also X-sectioned to verify no ELK delamination occurred. The ELK delamination seen on failing units of leg#5 did not always manifest itself as and open/short failure presumably because the damage occurs on a fine scale below the threshold of electrical test sensitivity.

Thermo-mechanical simulation results generated comparing BOC and BOL also substantiate the empirical data showing the stress relief manifested as a reduced bump strain (and hence correspondingly reduced stress in Si) by virtue of the BOL structure as has been published earlier [1].

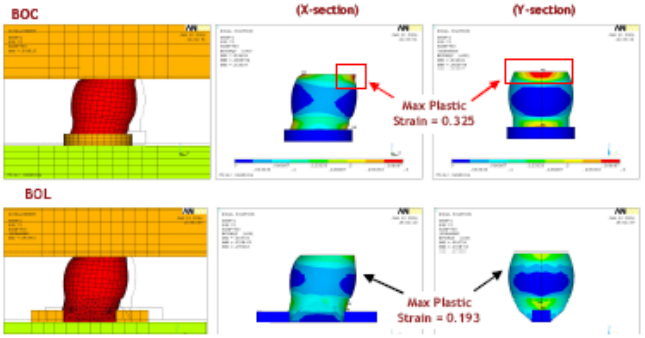


Fig. 6.6 FEM analysis comparing BOC & BOL structures

Subsequent reliability characterization was run to assess reliability robustness of the 45N-ELK test vehicle units and was completed successfully without any electrical failures or other forms of mechanical damage including ELK-delamination (Table 6.3).

Reliability test		EOL	MRT L3	Temp Cycle	
				500x	1000x
Sample Size	Leg#1/2/3/4	25ea / lot	22ea / lot	22ea / lot	22ea / lot
Results	O/S test	Pass(0/25)	Pass(0/22)	Pass(0/22)	Pass(0/22)
	T-SAM	Pass(0/25)	Pass(0/22)	Pass(0/22)	Pass(0/22)
	X-section (1ea/lot)	no abnormality (no ELK Delam /Bump crack)	no abnormality (no ELK Delam /Bump crack)	no abnormality (no ELK Delam /Bump crack)	no abnormality (no ELK Delam /Bump crack)

Table 6.3 – Reliability test results for 45N-ELK TV

7. Summary & Conclusions

We have demonstrated an innovative flip chip package structure termed "Low Cost Flip Chip" (LCFC) that (i) dramatically reduces package cost below that of conventional wire bond packages, and (ii) provides an interconnect structure which reduces stress on low K and ELK Si layers resulting in elimination of ELK damage. Key features of the LCFC package include a routing-efficient interconnect structure (no-SOP/BOL/Open SRO w/ Cu column bump) that enables routing of flip chip designs in low cost laminate substrates and an MUF assembly process using a high density matrix strip format. The new LCFC package is Pb-free and scalable to fine pitch providing seamless migration to future applications requiring 3D/TSV integration.

Acknowledgments

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